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Leon Brindley

Previous Work

Pragmatic Semiconductor **July 2023 - September 2023**
IC Design Intern Cambridge, UK
• Worked in Pragmatic's Emerging Applications (EA) Team at Cambridge Science Park for 13 weeks.
• Analogue and digital IC design using Cadence Virtuoso and Pragmatic's Helvellyn PDK for flexible electronics.
• Work included an accurate and compact SAR ADC containing either an R-2R or resistor-string DAC, along with its accompanying digital SAR logic, analogue comparator and level-shifter, as well as various other layouts.

Qualcomm Technologies **June 2022 - September 2022**
Interim Engineering Intern Cambridge, UK
• Further IC design (e.g. a low-power, low-area temperature sensor frontend) using Cadence Virtuoso in the Power Management Unit Team, having researched state-of-the-art academic papers through IEEEXplore.
• Performed various circuit simulations (e.g. DC, transient, safe operating area and Ansys Totem) for Qualcomm's next-generation voice and music cells, and presented the final results in design review presentations.
• Created clear and detailed documentation for all designs and tests in accordance with Qualcomm's standards.
• Completed an analysis of individual error contributions from Qualcomm's existing temperature sensor frontend, and how these would be affected by the subsequent signal processing circuitry and ADC.
• Used Atlassian Confluence/Jira and Microsoft Visio for teamworking and diagram design, respectively.

Qualcomm Technologies **June 2021 - September 2021**
Interim Engineering Intern Remote
• IC design (e.g. a low-frequency RC oscillator) using Cadence Virtuoso in the Power Management Unit Team.
• Performed circuit feasibility tests referencing academic papers from IEEEXplore and existing Qualcomm IP.
• Cell layout (e.g. a compact serpentine resistor) development and optimisation.

ArC Instruments **July 2020 - September 2020**
Undergraduate Intern Remote
• Developed a Python program (with a Qt5 GUI) for UDP-based RRAM experiments using the ArC ONE® Memristor Characterisation Platform.
• Tested UDP communication using a VPC in Dresden and documented the resultant bit error rate.
• Presented my work to the Centre for Electronics Frontiers (formerly at the University of Southampton).

Education

University of Cambridge **September 2024 - Present**
PhD in Physics Cavendish Laboratory

University of Cambridge **October 2023 - August 2024**
MRes in Sensor Technologies and Applications (**76%**) Chemical Engineering and Biotechnology

University of Southampton **September 2019 - June 2023**
MEng Electronic Engineering with Computer Systems (**78%**) Electronics and Computer Science

King Edward VI Five Ways **August 2012 - June 2019**
A-Level Mathematics (**A***) • A-Level Further Mathematics (**A***) • A-Level Physics (**A***) • A-Level Chemistry (**A***)
Level 3 Extended Project (**A***) • Eld Memorial Prize for Best Scholar

Scientific Societies

Cambridge Philosophical Society **December 2024 - Present**
Life Member Cambridge, United Kingdom

Institution of Engineering and Technology **February 2020 - Present**
Member (MIET) London, United Kingdom

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Previous Research

MRes Mini Research Project **December 2023 - April 2024**
Supervised by Dr Luca Sapienza Cambridge, UK

• Performed micro-photoluminescence experiments upon silicon nitride waveguides at the Nanoscience Centre.
• Learnt how to independently acquire and analyse readings from an electron-multiplying charge-coupled device (EMCCD) and reflection grating spectrometer (RGS).
• Qualitatively evaluated any sources of experimental error in the setup and researched the main barriers to commercialisation facing sensors based on photonic crystals.

MEng Group Design Project **September 2022 - January 2023**
Supervised by Dr Russel Torah Southampton, UK

• Project titled "Screen-Printed E-Textile Computer" in a team of four, with the University of Southampton's Smart Electronic Materials and Systems Research Group and Printed Electronics and Materials Laboratory.
• Researched the fundamental operational principles of organic electrochemical transistors (OECTs), the applications fulfilled by OECTs in academia and the future research required for commercially-viable OECTs.
• Developed layouts using L-Edit for modular components such as XOR gates, multiplexers and full adders using PEDOT:PSS-based OECTs. These can form a 4-bit bit-slice ALU with NOT, AND, ADD and SUB functions.
• Characterised different OECTs through characteristics such as transfer curves, ON/OFF drain current ratios and minimum switching voltages using an automated LabVIEW testbench.
• Designed a custom OECT LTspice model corresponding to the aforementioned characteristics with asymmetrical rise/fall times and adjustable leakage currents.
• Fabricated the designs using a DEK 248 screen printer and both UV and thermal curing.

Part III Individual Project **September 2021 - May 2022**
Supervised by Professor Geoff Merrett Southampton, UK

• Developed IoT smart tags for tracking PC component wear to facilitate a sustainable circular economy.
• Researched transistor wear mechanisms like electromigration, time-dependent dielectric breakdown and hot carrier injection. This included the fundamental methods of degradation, the effects of environmental conditions and computational load on the rate of degradation, and the extrapolation of each wear mechanism to estimate the extended lifetime and relative performance of the devices, with over 100 references cited using EndNote.
• Created IoT smart tags built around an Arduino Nano 33 BLE Sense, an SD card reader and an OLED display.
• Created an embedded Arduino program using C++ which acquires environmental data (including temperature, pressure and relative humidity), processes the acquired data and transmits packets via BLE. The program outputs data to an OLED screen for debugging and monitoring purposes, performs preliminary sanity checks on the acquired data and stores results locally before transmitting packets periodically to conserve battery.
• Created a hosted PC program using C++ and QML which receives packets via BLE, performs benchmarks (particularly CUDA-based matrix addition for GPUs) and analyses all available data to estimate component wear and performance scores. The program includes a GUI to support pairing with the smart tags and sharing the scores.

Academic Awards

Qualcomm UKESF Scholarship
UK Electronics Skills Foundation | Sponsored by Qualcomm Technologies

ECS Excellence Scholarship
University of Southampton | 1 of 3 Scholars in Electronics and Computer Science

Charles Belling IET Diamond Jubilee Scholarship
Institution of Engineering Technology & Belling Charitable Settlement | 1 of 3 Scholars Nationally

UKESF Scholar of the Year Award 2022 Runner-Up
UK Electronics Skills Foundation | Presented at TechWorks Awards and Gala Dinner

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Key Projects

Sensor Team Challenge (Team) Developed a semi-automated and non-invasive system for monitoring the biodiversity of farmland called DAISY, in collaboration with Rothamsted Research. DAISY captures geotagged photographs from cameras mounted on cattle, detects organic subjects (grass, clover, dung or bare soil) using several pre-trained machine learning models and presents the spatially resolved results in an online graphical user interface.
Sensor Design Project (Individual) Programmed and calibrated an accurate temperature sensor using an Arduino UNO R4 WiFi. For long-term data collection and viewing on battery power, an SD card reader and OLED display were connected using SPI and I^2C, respectively. Implemented an optical pulse meter using an LED, photodiode and transimpedance amplifier to detect light absorption by blood. Extracted the user's heart rate using both peak detection and SciPy's FFTpack module.
D2 Design Project (Team) Designed a ring oscillator, sequence detector and serial interface in S-Edit and L-Edit using TSMC's 0.18-micron CMOS process. The designs were initially checked using Tanner T-Spice and DRC/LVS checks, before being physically tested using custom test vectors once fabricated by TSMC.
D3 Design Project (Individual) Developed an analogue frontend circuit for a small weighing system composed of a full Wheatstone bridge of strain gauges and an instrumentation amplifier with a high CMRR.
ELEC6230: VLSI Systems Design (Individual) Designed a compact 3-input NOR gate using Magic VLSI and AMS' 0.35-micron process, with well-matched rise and fall times. Implemented a pseudo-random six-sided dice design in SystemVerilog. Designed and characterised a full adder using Magic VLSI and TSMC's 0.18-micron process, with a compact gate matrix design. Created an 8-bit divider with a bit-slice datapath using Magic VLSI and a synthesisable SystemVerilog control unit.
ELEC6231: VLSI Design Project (Team) Developed a custom cycle computer chip using UMC's 0.18-micron process. This included a high-level SystemVerilog behavioural model for the simulation and synthesis of the design, followed by a full layout with scan path testability. Explored the full chip design flow (involving stages like clock tree synthesis, place-and-route and Tcl scripting), as well as Power-Performance-Area (PPA) optimisation. The base cycle computer design (containing an odometer, trip timer, speedometer, cadence meter and four seven-segment displays) was extended by adding an altimeter and OLED display.
ELEC6234: Embedded Processors (Individual) Designed an application-specific embedded processor that implements an affine transformation algorithm. The MIPS-inspired RISC design linked together distinct SystemVerilog modules (such as an instruction decoder, registers, ALU and top-level CPU). Finally, the processor was synthesised and demonstrated using the Terasic DE1-SoC FPGA Development Kit.

Key Skills

Organic Electronics • OECTs • Cleanroom Fabrication • Device Characterisation • AutoCAD • LabVIEW
Physics • Chemistry • Mathematics • Cadence Virtuoso • Intel Quartus Prime • Circuit Analysis
C++/C/Embedded C • SystemVerilog • Tcl Scripting • LaTeX • Computer Architecture • Control Theory
Laboratory Skills • Time Management • Leadership • Teamworking • Public Speaking • Problem Solving

Recent Voluntary Activities

Gonville and Caius College MCR **October 2023 - Present**
Computing Officer Cambridge, UK
University of Southampton IET On Campus **October 2021 - June 2023**
President Southampton, UK
Student Scout and Guide Organisation **March 2021 - April 2023**
National Publicity Officer National, UK
University of Southampton Electronics and Computer Science Society **March 2020 - April 2021**
Events Officer Southampton, UK